IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) An apparatus comprising:

a first processor that includes a first processor element; and

a second processor that includes a second processor element, wherein the first processor is configured to transmit data to the second processor through a third processor, wherein no processor element within the third processor is configured to perform a process operation on the data as part of the transmission of the data from the first processor to the second processor, wherein the first processor includes a type of hardware accelerator that is not included in the second processor.

2. (Original) The apparatus of claim 1, wherein the first processor is not directly connected with the second processor.

3. (Original) The apparatus of claim 1, wherein no processor element within the third processor is involved in the transmission of data from the first processor to the second processor through the third processor.

4. (Original) The apparatus of claim 1, wherein the first processor, the second processor and the third processor are coupled together in a point-to-point configuration.

5. (Currently Amended) An apparatus comprising:

a first processor that includes a first processor element that is configured to perform a first data process operation; and

a second processor that includes a second processor element that is configured to perform a second data process operation based on an output from the first data process operation, the first processor to transmit the output from the first data process operation to the second processor based on a logical connection that includes traversal through a port ring of a third processor, wherein a third processor element within the third processor is not configured to perform a data

process operation between the first data process operation and the second data process operation, wherein the first processor includes a type of hardware accelerator that is not included in the second processor and wherein the first processor element in the first processor is configured to perform the first data process operation on data streams received into the expansion interface at least simultaneously in part with second data process operation performed by the second processor element in the second processor.

6. (Original) The apparatus of claim 5, wherein the first processor, the second processor and the third processor are part of a number of processors that are in a point-to-point configuration.

7. (Canceled)

8. (Original) The apparatus of claim 5 further comprising,

an expansion interface to receive data on which the processor element in the first processor is to perform the first data process operation; and

a memory interface unit coupled to a memory that is external to the apparatus, wherein the memory is configured to store an output of the second data process operation.

9. - 18. (Canceled)

19. (Currently Amended) A method comprising:

receiving a stream of data in a first processor having a first processor element;

performing, by the first processor element, image processing operations on at least a part of the stream of data; and

transmitting a result of the image processing operations to a second processor through a third processor having a third processor element, independent of image processing operations by the third processor element, wherein the first processor includes a type of hardware accelerator that is not included in the second processor.

20. (Original) The method of claim 19, wherein transmitting the result of the image processing operations to the second processor through the third processor includes transmitting the result of the image processing operations to the second processor through a logical connection that includes transmission through a series of processors including the third processor.

21. (Original) The method of claim 19, wherein receiving the stream of data in the first processor having the first processor element includes receiving the stream of data in the first processor having the first processor element at least simultaneously in part with performing, by a second processor element in the second processor, a different image processing operation.

22. (Currently Amended) A method comprising:

performing, by a hardware accelerator in a first image signal processor within a multi-processor point-to-point configuration, the following operations until receipt of image data from an image scanning operation is complete,

executing, by a first processor element in the first image signal processor, an image process operation on the image data; and

transmitting a result of the image process operation to a second image signal processor within the multi-processor point-to-point configuration through a logical connection that includes a number of ports of a number of other different image signal processors within the multi-processor point-to-point configuration, wherein a type of the hardware accelerator is not included in at least one of the number of other different image signal processors.

23. (Original) The method of claim 22, wherein transmitting the result of the image process operation to the second image signal processor includes transmitting the result of the image process operation to the second image signal processor through the logical connection, wherein other processing elements in the other different image signal processors do not process the image data prior to processing by a second processor element in the second image signal processor.

24. (Original) The method of claim 22 further comprising receiving the image data from a source that is external to the multi-processor point-to-point configuration.

25. (Currently Amended) A machine-readable storage medium that provides instructions, which when executed by a machine, cause said machine to perform operations comprising:

receiving a stream of data in a first processor having a first processor element;

performing, by the first processor element, image processing operations on at least a part of the stream of data; and

transmitting a result of the image processing operations to a second processor through a third processor having a third processor element, independent of image processing operations by the third processor element, wherein the first processor includes a type of hardware accelerator that is not included in the second processor.

26. (Currently Amended) The machine-readable storage medium of claim 25, wherein transmitting the result of the image processing operations to the second processor through the third processor includes transmitting the result of the image processing operations to the second processor through a logical connection that includes transmission through a series of processors including the third processor.

27. (Currently Amended) The machine-readable storage medium of claim 25, wherein receiving the stream of data in the first processor having the first processor element includes receiving the stream of data in the first processor having the first processor element at least simultaneously in part with performing, by a second processor element in the second processor, a different image processing operation.

28. (Currently Amended) A machine-readable storage medium that provides instructions, which when executed by a machine, cause said machine to perform operations comprising:

recursively performing, by a hardware accelerator in a first image signal processor within a multi-processor point-to-point configuration, the following operations until receipt of image data from an image scanning operation is complete,

executing, by a first processor element in the first image signal processor, an image process operation on the image data; and

transmitting a result of the image process operation to a second image signal processor within the multi-processor point-to-point configuration through a logical connection that includes a number of ports of a number of other different image signal processors within the multi-processor point-to-point configuration, wherein a type of the hardware accelerator is not included in at least one of the number of other different image signal processors.

29. (Currently Amended) The machine-readable storage medium of claim 28, wherein transmitting the result of the image process operation to the second image signal processor includes transmitting the result of the image process operation to the second image signal processor through the logical connection, wherein other processing elements in the other different image signal processors do not process the image data prior to processing by a second processor element in the second image signal processor.

30. (Currently Amended)The machine-readable storage medium of claim 28 further comprising receiving the image data from a source that is external to the multi-processor point-to-point configuration.